REMARKS

This is a timely reply to the Final Official Action of August 27, 2002. Included with this reply is a Request for Re-examination (RCE) and associated fees for a one-month extension of time. In the Official Action the Examiner rejects pending claims 1-8 and 15-17 and 19-22 of the application. The grounds for rejection are traversed below.

Support for new claims 23-26

Support for new claims 23-26 can be found in the second full paragraph on page 5 of the present application.

Claims 1-8, 15-22 remain in the application. New claims 22-26 have been added to the application. The application now comprises 5 (five) independent claims and 20 total claims. The application, as previously amended, comprised 5 (five) independent claims and 16 (sixteen) total claims. Therefore, no excess claim fees are due.

Claim 22

In the Advisory Action, the Examiner notes that the proposed new limitation in claim 22 appears to change the scope of the claims and that this would require further consideration and/or search.

Applicant's respectfully disagree with the position taken by the Examiner. The change made to claim 22 was only to clarify which "selected ones" were connected with buried conducting channels and which "selected ones" were not connected with buried conducting channels. However, since the amendment to claim 22 was not entered. Applicant's resubmit the amendment to claim 22.

Claim 22 has been amended to recite additional selected ones of the plurality of spaced apart regions. By adding the term "additional," we hope to clarify that the additional selected ones of the plurality of spaced-apart regions in claim 22 are not the same selected ones of the plurality of spaced-apart regions in claim 19.

Further, Applicant's submit that claim 22 is directed toward patentable subject matter as claim 22 is directed toward the same subject matter as old dependent claim 18. Dependant claim 18 was deemed to be directed toward patentable subject matter by the Examiner in his Office Action dated August 27, 2002.

35 USC § 103(a) - Rejection based on Choi (U.S. Patent No. 6,215,158)

Claim 1

In the Official Action the Examiner rejects the claims of the application under 35 U.S.C. 103 as being unpatentable over U.S. Patent No. 6,215,158 to Choi. Specifically, the Examiner asserts that Choi teaches all of the elements found in claim 1 and the recitations of "a camouflaged interconnection" and "in a manner which inhibits reverse engineering thereof" in the claim preamble are treated as non-limiting.

As noted by MPEP 2143.03, to establish a *prima facie* case for obviousness, all the claim limitations must be taught or suggested by the prior art. The Applicant respectfully asserts that Choi does not teach all of the claim limitations of claim 1.

The Examiner takes the position on page 7 of the Official Action regarding camouflaging that "the Choi reference provides the same structure as is claimed; therefore, if it is true in the present invention then it is also true in the Choi reference." Applicant respectfully disagrees that the Choi reference provides the same structure as claimed. Choi teaches in col. 3, lines 37-42 "The dielectric 190 has been patterned with openings 240, 250 to expose a portion of the first and second source regions 140, 150 respectively. A high energy beam of n-dopant may now be used to create implanted plugs 231, 232 thereby forming connections between the interconnect layer 130 and the first and second source regions 140, 150." In col. 3, lines 54-55, Choi teaches "Conductive plugs 440, 450, 460 are deposited using conventional techniques to fill the openings 240, 250, 360, respectively." Choi further teaches in col. 3, lines 58-67 that "Conductive plug 460 will ultimately provide a conventional contact for drain region 160. However, conductive plugs 440, 450 are dummy plugs, which are not to be used for contacting other parts of the semiconductor, but rather are simply used to fill the openings 240, 250 remaining after the formation of the implanted plugs 231, 232. Further connection of the first and second source regions 140, 150 to other parts of the semiconductor will be accomplished by connecting the interconnect layer 130 through a connection not shown." We submit that the conductive plugs 440, 450, 460 are present only for two purposes. One purpose, which is served by conductive plug 460, is to provide a conventional contact. The second purpose, which is served by conductive plugs 440, 450, is to provide a contact to the underlying interconnect layer 130. Thus, a reverse engineer will see the conductive plugs 440, 450 which are not used for contacting other parts of the semiconductor and would immediately infer that a

connection has been made via the interconnect layer 130. Therefore, we submit that the interconnection scheme of Choi is not camouflaged at all.

For the reasons stated above, claim 1 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 2-4 and 23 are also deemed patentable over the cited prior art through at least their dependency on claim 1.

The Examiner takes the position that, without reading the specification of Choi, a reverse engineer would not know that there exists a buried interconnect layer 130 deep below and inside the substrate, allegedly camouflaged by the other layers above. The Examiner further asserts that the reverse engineer would not know how and which source/drain regions are connected to each other by the interconnect layer 130 because not all source/drain regions in devices are connected to each other.

The Examiner cites the drawings of Choi against the claims because he finds it convenient to do so but seeks to ignore the written description of Choi and the other drawings of Choi because he finds the these other sections of Choi inconvenient since the other drawings and the written specification clearly teach away from Applicant's invention.

The interesting point is why does the Examiner decide that he can only rely on a portion of Choi's disclosure? Clearly the reason is that the Examiner has had the privilege of reading Applicant's patent application and, upon reviewing the claims, the Examiner then uses an after-the-fact analysis to try to read the claims on only a portion of the Choi disclosure. However, the real test of whether or not something is disclosed by the prior art is what does the prior art document teach to a person of ordinary skill in the art who is not familiar with Applicant's invention. This person does not know, in advance, that they should only look at certain figures of Choi and ignore the other figures, and, moreover, ignore the written disclosure. Indeed, where is there anything in Choi which would tell a person of ordinary skill in the art that they should only pay attention to certain portions of the Choi disclosure and ignore other portions? Since the Examiner has not been able to point to any such disclosure, it is believed that it does not exist. Indeed, it is believed that the only reason that the Examiner points to certain portions of the Choi disclosure that he finds convenient to cite against the claims and ignores other portions of the Choi disclosure, which he finds inconvenient to cite in his prior art

analysis, is that the Examiner is clearly using a hindsight approach to Applicant's claims when citing the Choi document.

Additionally, the Examiner's analysis also seems to assume that the structure of the Choi device has been manufactured. While the Applicants believe that point is irrelevant (see below), it is noted that if the Examiner is aware of facts which he is using to reject the claims, then the Examiner is required to submit an Affidavit under 37 C.F.R. 1.104(d)(2). The Examiner is respectfully requested to produce the Affidavit required by this rule. For if the Choi device has been manufactured, on what date was it first manufactured? If it were manufactured after the filing date of the present application, then how would the Examiner use such manufacture as a novelty-barring event?

Finally, even assuming that the Choi device has been previously manufactured, what would entitle the Examiner to ignore the teachings of the Choi patent? Clearly, the Examiner finds the written disclosure of Choi to be inconvenient in his prior art analysis and therefore the Examiner would just as soon ignore the inconvenient portions of the Choi disclosure. However, it is clear that the only reason that the Examiner is doing this is because he is using an after-the-fact analysis of Applicant's claims. A person of ordinary skill in the art who is familiar with the Choi disclosures, whatever they might be, would not have the benefit of knowing, in advance, what portions of the Choi disclosures to consider and what portions of the Choi disclosure to ignore. It is only the Examiner who is able to do that and that is only because the Examiner has read the present patent application.

Further, Applicants will be submitting an affidavit attesting to the fact, that even if the Choi patent has been reduced to practice, the reverse engineer would easily discern the purpose of the two dummy plugs 440, 450. If the Examiner does not have the affidavit in the file with this RCE, the Applicant respectfully requests that the Examiner call the Applicant's representative so the Applicant's representative can insure that the Examiner receives a copy of the affidavit.

Claim 5

As noted by MPEP 2143.03, to establish a *prima facie* case for obviousness, all the claim limitations must be taught or suggested by the prior art. The Applicant respectfully asserts that Choi does not teach all of the claim limitations of claim 5.

Claim 5 claims "at least one implanted region of opposite conductivity type being disposed over at least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" (emphasis added). As discussed above, the structure of Choi does not camouflage the at least a majority of said plurality of interconnects. The Examiner is asked to point out where in Choi "at least one implanted region of opposite conductivity type being disposed over at least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" is taught or suggested.

Therefore, for the reasons stated above, claim 5 is clearly distinguishable over Choi, and thus deemed to be patentable. In addition, claims 6-8 and 24 are also deemed patentable over the cited prior art through at least their dependency on claim 5.

Claim 15

Claim 15 recites, " An interconnection scheme for interconnecting two spaced-apart regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising: a first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type, the first region providing a buried conducting channel for the two spaced-apart regions; and a second region of opposite conductivity type in the integrated circuit or device, said second region overlaying said first region to conceal the conducting channel." (emphasis added)

Choi does not disclose a "second region overlaying said first region to conceal the conducting channel".

In order to show that the present invention, as claimed in claim 15, is obvious in view of Choi, the Examiner must show how Choi teaches all of the limitations in claim 15. In the Advisory Action, the Examiner asserts that Choi teaches the second region 121 overlying a portion of the conducting channel. However, this does not address how the

second region overlying said first region conceals the conducting channel. Thus, the Examiner is requested to show how the second doped region 121 of Choi conceals the interconnect layer 130, 232, 233. Unless the Examiner can show how Choi teaches each and every element, claim 15 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 16-17 and 25 are also deemed patentable over the cited prior art through at least their dependency on claim 15.

Claim 19

Claim 19 recites, "A interconnection scheme for interconnecting a plurality of spaced-apart regions of a common conductivity type in an integrated circuit or device, the interconnection scheme comprising: a plurality of buried conducting channels, each buried conducting channel being of the common conductivity type, each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions, each buried conducing channel providing an electrical connection between said selected ones of the plurality of spaced-apart regions; and at least one region of an opposite conductivity type in the integrated circuit or device, the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels." (emphasis added)

For reasons similar to those provided in support for the patentability of claims 1, 5 and 15, Choi does not disclose "the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels".

The Examiner is asked to point out where in Choi "the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels" is taught or suggested.

We submit that claim 19 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 20-22 and 26 are also deemed to be patentable over the cited prior art through at least their dependency on claim 19.

Claim 18

The Applicants wish to thank the Examiner for his indication that claim 18 is directed toward patentable subject matter in his Office Action of August 27, 2002. In the Supplemental Advisory action, the Examiner indicated that he entered the amendment to claim 18 made by the Applicant in the Response dated October 24, 2002. However, in the Supplemental Advisor action, the Examiner did not indicate that claim 18 was allowed, instead the Examiner stated that claim 18 was under objection. Applicants believe that this was an oversight by the Examiner and that claim 18 (amended as an independent claim) should be deemed allowable over the cited prior art.

Claims 23-26

Dependent claims 23-26 are directed toward the feature that the depth of the region overlying the buried channel is less than the depth of the buried channel. Applicant is unaware of where in Choi this feature is taught disclosed or suggested. Thus, claims 23-26 are deemed to be patentable.

Conclusion

Hence, the Applicant respectfully submits that all claims of the application are patentable over the cited references. In view of the above, reconsideration and allowance of the pending claims are respectfully solicited.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231 on

December 23, 2002
(Date of Deposit)

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APPENDIX A

22. (Once Amended) The interconnection scheme of claim 19 further comprising at least one other region of the opposite conductivity type, the at least one other region of the opposite conductivity type being laterally disposed of and in direct contact with additional selected ones of the plurality of spaced-apart regions, wherein said additional selected ones of the plurality of spaced-apart regions are not electrically connected by one of said plurality of buried conducting channels.